In the Claims:

Claims 1, 3, 4, 13, 14, 16, 18, 19, 26, and 29 are canceled. Claims 2, 5, 6-11, 15, 17, 20-25, 27, 28, and 30 are amended. Claims 30 and 31 are new. The claims are as follows:

1. (Canceled)

2. (Currently Amended) The semiconductor device of claim [[1]] 5, wherein each of the local memory structures in each said system comprises a first address space that is shared with the processing devices in the other systems, and wherein each of the local memory structures in each said system comprises a second address space that is not shared with the processing devices in any of the other systems.

3-4. (Canceled)

5. (Currently Amended) ~~The semiconductor device of claim 4~~ A semiconductor device, comprising:

a plurality of systems within the semiconductor device, each system comprising at least one processing device and a local memory structure, wherein each said processing device is electrically coupled to each said local memory structure within each said system, wherein each said local memory structure is electrically coupled to each of the remaining local memory structures, wherein each said local memory structure is adapted to share address space with each of said processing devices, wherein each said processing device is adapted to transmit data and

instructions to each said local memory structure, wherein each said processing device is further adapted to retrieve data and instructions from each said local memory structure, wherein each said local memory structure comprises a memory device coupled to a memory control device, wherein each said memory control device is adapted to control a flow of said data and instructions between each processing device and each memory device, wherein each said memory device comprises a decoder and a read queue, wherein a decoder in a first system within the plurality of systems is adapted to accept data and instructions from a second system within the plurality of systems and transmit the data to both a memory device and a read queue in the first system, and wherein a processing device in the first system is adapted to read the data from the read queue of the first system instead of from the memory device of the first system if the second system is transmitting the data to a memory location in the memory device at same time as the processing device is trying to read the data from the memory location.

6. (Currently Amended) The semiconductor device of claim [[4]] 5, wherein [[the]] each said memory device is selected from the group consisting of, random access memory, read only memory, and erasable programmable read only memory.

7. (Currently Amended) The semiconductor device of claim [[1]] 5, wherein each said system is adapted to transmit a memory write message to each of other said systems.

8. (Currently Amended) The semiconductor device of claim [[1]] 5, wherein each said local memory structure is electrically coupled to each of the remaining local memory structures with a

high speed serial link.

9. (Currently Amended) The semiconductor device of claim [[1]] 5, wherein a physical distance between each said processing device and each said local memory structure within each said system is in a range of about 50 microns to about 400 microns.

10. (Currently Amended) The semiconductor device of claim [[1]] 5, wherein each said processing device is selected from the group consisting of a central processing unit and a digital signal processor.

11. (Currently Amendedl) The semiconductor device of claim [[1]] 5, wherein the plurality of systems is adapted to maintain data coherency between each of said memory structures and each of said processing devices.

12. (Original) The semiconductor device of claim 11, wherein said data coherency is maintained using a protocol selected from the group consisting of contention, token passing, and polling.

13-14. (Canceled)

15. (Currently Amended) A semiconductor device, comprising:

a plurality of systems within the semiconductor device, each system comprising a plurality of processing devices and a local memory structure, wherein each processing device of

each said plurality of processing devices is electrically coupled to each said local memory structure within each said system, wherein each said local memory structure is electrically coupled to each of the remaining local memory structures, wherein each said local memory structure is adapted to share address space with each of said processing devices, wherein each said processing device is adapted to transmit data and instructions to each said local memory structure, wherein each local memory structure comprises a memory device coupled to a memory control device, and wherein the memory control device is adapted to control a flow of said data and instructions between each of the plurality of processing devices and each said memory device ~~The semiconductor device of claim 14~~, wherein each memory control device in each system comprises a decoder and a read queue, wherein the decoder is adapted to accept data and instructions from a first processing device within the plurality of processing devices within a system and transmit the data and instructions to both the memory device and the read queue in the system, wherein a second processing device in the system is adapted to read the data and instructions from the read queue instead of the memory device if the first processing device is transmitting the data and instructions to a memory location in the memory device at same time as the second processing device is trying to read the data and instructions from the memory location.

16. (Canceled)

17. (Original) The method of claim [[16]] 20, wherein each of the local memory structures in each said system comprises a first address space that is shared with the processing devices in the

other systems, and wherein each of the local memory structures in each said system comprises a second address space that is not shared with the processing devices in any of the other systems.

18-19. (Canceled)

20. (Currently Amended) A method for controlling data flow, comprising:

providing a plurality of systems within a semiconductor device, each system comprising at least one processing device electrically coupled to a local memory structure;

electrically coupling each of said local memory structures to each of the remaining local memory structures;

sharing, by each local memory structure in each said system, address space with each of the processing devices in each of the other systems;

transmitting, by each said processing device, data and instructions to each said local memory structure;

retrieving by each said processing device, data and instructions from each said local memory structure, wherein each local memory structure comprises a memory device coupled to a memory control device;

controlling, by each said memory control device, a flow of data and instructions between each processing device and each memory device ~~The method of claim 19~~, wherein each memory device comprises a decoder and a read queue;

accepting, by a decoder in a first system within the plurality of systems, data and instructions from a second system within the plurality of systems; and

transmitting, by the decoder, the data and instructions to both a memory device and a read queue in the first system, wherein a processing device in the first system is adapted to read the data and instructions from the read queue instead of the memory device if the second system is transmitting the data and instructions to a memory location in the memory device at same time as the processing device is trying to read the data and instructions from the memory location.

21. (Currently Amended) The method of claim [[19]] 20, wherein each said [[the]] memory device is selected from the group consisting of, random access memory, read only memory, and erasable programmable read only memory.

22. (Currently Amended) The method of claim [[16]] 20, further comprising;

transmitting, by each said system, a memory write message to each of other said systems.

23. (Currently Amended) The method of claim [[16]] 20, wherein each said local memory structure is electrically coupled to each of other said local memory structures with a high speed serial link.

24. (Currently Amended) The method of claim [[16]] 20, wherein a physical distance between each said processing device and each said local memory structure within each said system is in a range of about 50 microns to about 400 microns.

25. (Currently Amended) The method of claim [[16]] 20, wherein each said processing device is

selected from the group consisting of a central processing unit and a digital signal processor.

26. (Canceled)

27. (Currently Amended) The method of claim [[26]] 30, wherein said data coherency is maintained using a protocol selected from the group consisting of contention, token passing, and polling.

28. (Currently Amended) The method of claim [[16]] 20, wherein each system comprises a plurality of processing devices electrically coupled to each said local memory structure within each said system.

29. (Canceled)

30. (Currently Amended)

A method for controlling data flow, comprising:

providing a plurality of systems within a semiconductor device, each system comprising at least one processing device electrically coupled to a local memory structure;

electrically coupling each of said local memory structures to each of the remaining local memory structures;

sharing, by each local memory structure in each said system, address space with each of the processing devices in each of the other systems;

transmitting, by each said processing device, data and instructions to each said local memory structure;

maintaining, by the plurality of systems, data coherency between each of said memory structures and each of said processing devices, wherein each sai9 local memory structure comprises a memory device coupled to a memory control device;

controlling, by each said memory control device, a flow of data and instructions between each of the plurality of processing devices and each memory device within each system

~~The method of claim 29~~, wherein each memory control device in each system comprises a decoder and a read queue;

accepting, by a decoder in a first system within the plurality of systems, data and instructions from a processing device within the plurality of processing devices in the first system within the plurality of systems;

transmitting by the decoder the data and instructions to both the memory device and the read queue in the system; and

reading by a second processing device in the system the data and instructions from the read queue instead of the memory device if the first processing device is transmitting the data and instructions to a memory location in the memory device at same time as the second processing device is trying to read the data and instructions from the memory location.

31. (New) The semiconductor device of claim 8, wherein each high speed serial link is selected from the group consisting of a universal serial bus (USB) and a peripheral component interconnect (PCI).

31. (New) The method of claim 23, wherein each high speed serial link is selected from the group consisting of a universal serial bus (USB) and a peripheral component interconnect (PCI).